Performance evaluation of full adder

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Abstract: *This paper presents different techniques of one bit Full adder. In every technique the main requirements are power consumption, speed and power delay product. The proposed FIN-FET technique gives the bette.r power consumption, speed and power delay product than other techniques. The proposed Fin-FET technique is compared with some of the popular adders based on the power consumption, speed and power delay product. We designed each of these techniques by using Spice simulation soft wares.*
Keywords: *Full Adder, CMOS, TG, CPL, GDI, FIN-FET.*

I. Introduction

The rapid growth in the portable devices demands the less power consumption, better speed and power delay product. Another requirement of these technologies is Area. Digital Signal processor (DSP) is the heart of the several Portable Electronics devices.Which performs the several tasks like image processing, video processing, Fast Fourier Transforms (FFT) and so on. To perform these kind of operations DSP uses a fundamental operation i.e addition. The addition operation plays most prominent role in the DSP operations. So enhancing the performance of the addition operation will leads to good performance of the hole system.This paper is discussing about several techniques of full adder. Each of these techniques have their own advantages and disadvantages.

II. Full Adder

A full adder is a combinational circuit which performs addition among the three bits.Sum and carry are the outputs of the full adder circuit. Here we have analysed the full adder using NOT gate, AND gate, and XOR gate. The figure shows the Full Adder circuit with different logic gates.
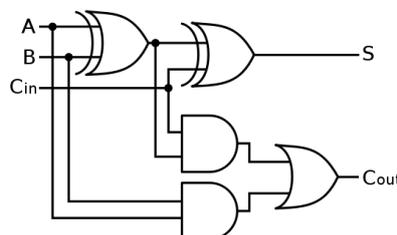
Fig.1 Full Adder using logic gates

Truth table of Full Adder

A	B	C	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

III. Full Adder Using CMOS

Complementary metal-oxide-semiconductor abbreviated as CMOS, is a technology for constructing integrated circuits. CMOS technology is widely used for several analog circuits such as data convertors, image sensors and highly integrated transceivers. CMOS uses symmetrical and complementary pairs of n-type and p-type metal oxide semiconductor field effect transistor (MOSFETs) for logic functions. PMOS gets on when the input is low (0) and NMOS gets on when the input is high (1).
High noise immunity and low static power consumption are the two important characteristics of CMOS devices. Heat dissipation is low in CMOS circuits when compared to other forms of logic circuits. The circuit diagram of full subtractor using CMOS is shown in figure.
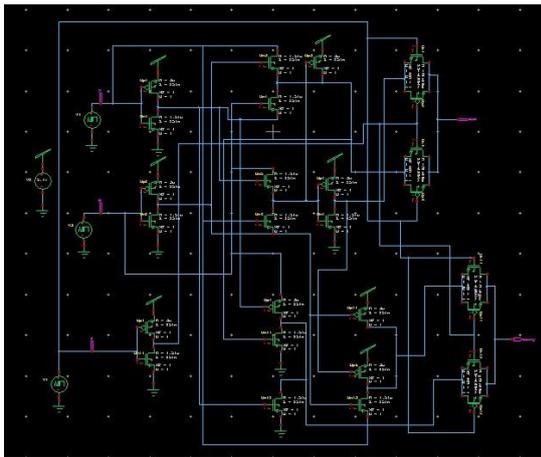
Fig. Schematic Diagram of Full adder(CMOS)
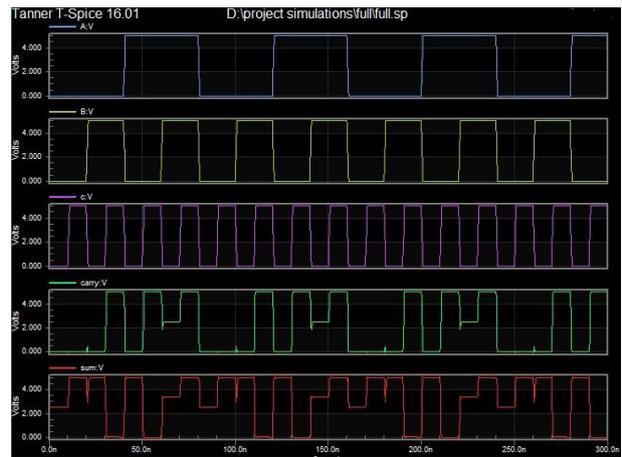
Fig . Out put Wave forms

IV. Full Adder Using CPL

The complex logics can be alternatively implemented using CPL(complementary pass transistor logic). CPL is extremely fast and efficient. Some of the examples of CPL circuits are shown in figure 5.
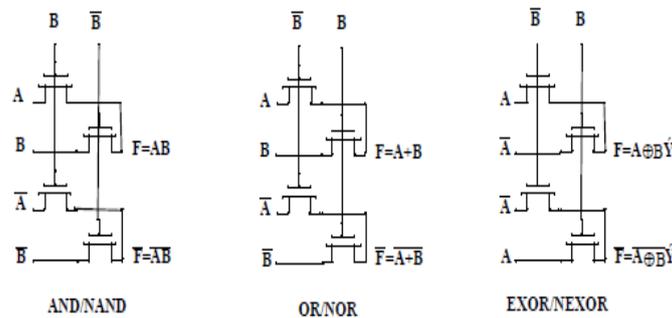
Fig. Realization of Logic Gates using CPL method

By eliminating the redundant transistors, it reduces the count of transistors used to make different logic gates. In order to pass logic levels between nodes of a circuit the transistors are used as switches. The main principle involved in CPL is the use of NMOS pass transistor for logic organisation and elimination of the PMOS latch. The circuit diagram of full adder using CPL is shown in figure.
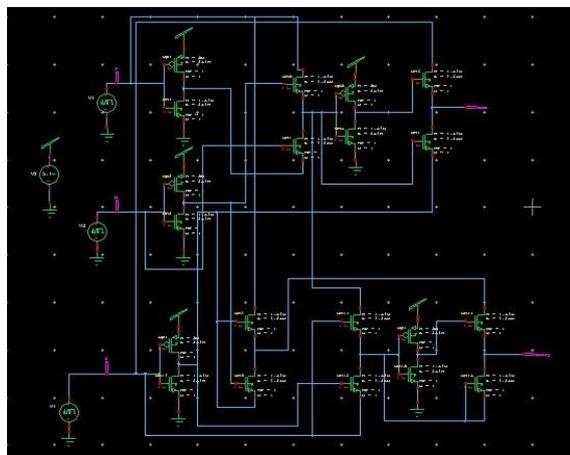
Fig. Schematic Diagram of Full adder (CPL)

Fig. Output Wave forms of CPL method

V. Full Adder Using GDI

GDI(gate diffusion input) is a technique of low power digital circuit design which reduces power consumption, delay and area. It is based on the use of a simple cell as shown in figure. It is similar to that of CMOS invertor but there are some differences:GDI cell contains three inputs. They are G(common gate input of NMOS and PMOS), P(input to the source/drain of PMOS) and N(input to the source/drain of NMOS).
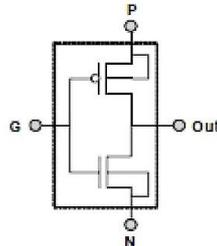
Fig.GDI cell

GDI technique allows implementation of a wide range of complex logic functions using only two transistors. This method produces designs which are fast with low power dissipation by using less number of transistors. The circuit diagram of full subtractor using GDI technique is shown in figure 8.
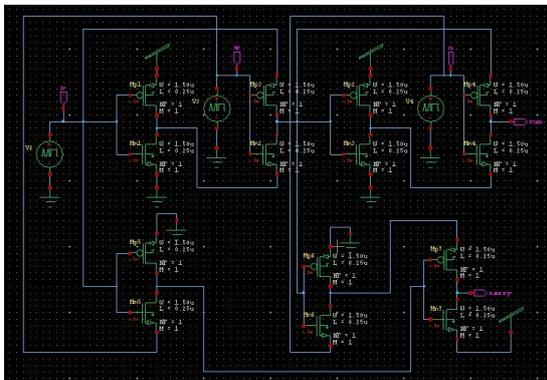
Fig. Schematic Diagram of Full Adder (GDI)
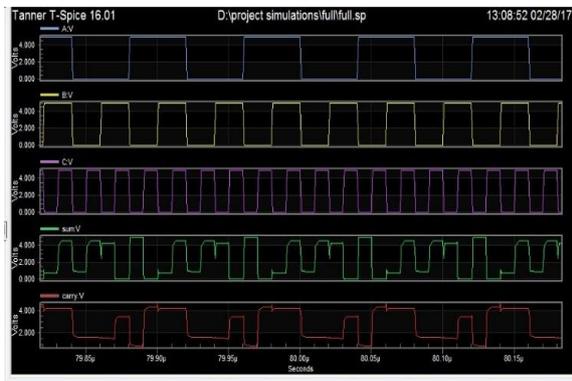
Fig. Output Wave forms of the GDI Technique

VI. Full Adder Using Finfet

Conventional MOSFETs have inherent problems of large leakage currents from gate to channel and increasingly unreliable transistor characteristics. To cater these problems, FinFET transistor technology has been developed which has cast a profound impact on the semiconductor industry. It provides a new pathway for Moore's Law beyond 20nm as they have much better performance and reduced power consumption compared to planar transistors.

The next few years should be very interesting as the benefits of this technology are seen in products from smart phones to servers.

The below figures shows the FinFET layout diagrams.
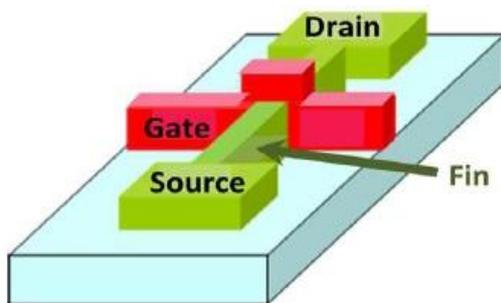
Fig: FinFET Layout
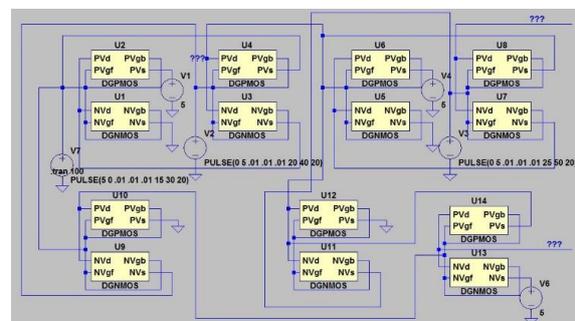
Fig: Schematic view of Full adder using FinFET

The Full adder using the FinFET is shown above and it shown the lower power consumption when compared to the CMOS logic.

VII.   Comparison Of Different Full Adder Techniques

We have designed full adder in different techniques. Each technique has its own advantages and disadvantages. Below table shows the comparison of all these techniques.

Table. Power consumed by each Technique

Technique	Power consumption(W)
CMOS	6.474195e-003
GDI	4.242147e-004
CPL	1.900524e-003
FinFET	190.9uw

VIII.   Conclusion

From the table which is show above gives the complete Performance Evolution of the Full adder. Finally we can conclude that FinFET technique is best technique in terms of the power consumption. It consumes and dissipates less power.

Acknowledgment

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